

AMENDMENTS TO THE CLAIMS

Please amend claims 1-3, 10, 12, 14, 15-17, 19, 21-23, 43 and 54 and cancel claims 4-9, 26-39, 46-53 and 59-61 without prejudice or disclaimer of the underlying subject matter as set forth below:

1. (CURRENTLY AMENDED) A digital-analog converter circuit for converting an n-bit (n is an integer of 2 or more) digital data signal comprising 2^n step select units connected across 2^n reference voltage lines, each step select unit including n serially connected analog switches polarized to match the a logic state of each data signal n-bit (n is an integer of 2 or more), and $2n$ tone select units respectively connected across the outputs of each of the $2n$ reference voltage lines bit of the n-bit digital data signal.

2. ((CURRENTLY AMENDED) A digital-analog converter circuit as claimed in claim 1 ~~comprising one conductive type MOS transistor~~, wherein each of said n analog switches ~~corresponds to the logic of each bit of said data signal~~ comprises a conductive-type MOS transistor.

3. (CURRENTLY AMENDED) A digital-analog converter circuit as claimed in claim 2, wherein the ~~amplitude of said n-bit digital data signal is~~ has a low by an amount amplitude equal to the a reference voltage minimum less a threshold value of the a P-channel MOS transistor in the reference voltage level range and is a high by an amount amplitude equal to the a reference voltage maximum plus a threshold of the an N-channel MOS transistor.

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9. (CANCELED).

10. (CURRENTLY AMENDED) A level shift circuit ~~having a CMOS latch cell as the basic structure and~~ for converting a low voltage amplitude signal to a high voltage amplitude signal comprising:

a CMOS latch cell having two input sections,

wherein a first resistor element is inserted ~~respectively between each of the two signal sources and the two input sections of said CMOS latch cell and two~~ signal sources.

11. (ORIGINAL) A level shift circuit as claimed in claim 10, wherein said first resistor element is a transistor.

12. (CURRENTLY AMENDED) A level shift circuit as claimed in claim 10, wherein a second resistor ~~elements~~ element ~~is the~~ are inserted between ~~the~~ a power supply and each of the two input sections of said CMOS latch cell.

13. (ORIGINAL) A level shift circuit as claimed in claim 12, wherein said first resistor element and said second resistor element are transistors.

14. (CURRENTLY AMENDED) A level shift circuit as claimed in claim 12, wherein level shift operation is performed only when ~~said~~ a switch is in an on status by utilizing switches having a finite resistance value as said first and said second resistor elements, and at all other times latch operation is performed.

15. (CURRENTLY AMENDED) A level shift circuit as claimed in claim 14, wherein said level shift circuit has a control circuit to set the switch to the on status only when necessary.

16. (CURRENTLY AMENDED) A level shift circuit as claimed in claim 14, wherein said level shift circuit has a reset circuit to determine ~~the~~ an initial status of said CMOS latch cell.

17. (CURRENTLY AMENDED) A shift register comprising a plurality of transfer stages and having a first level shift circuit to supply a start signal as a level shift to ~~the~~ a first stage of the transfer stages and a second level shift circuit to supply a clock signal as a level shift to each of the transfer stages, wherein said first and second level shift circuits ~~have~~ include a CMOS latch cell ~~as the basic structure having two input sections~~ and a first resistor element is inserted ~~respectively~~ between each of the two input sections and ~~the~~ two input signal sources ~~of said CMOS latch cell~~.

18. (ORIGINAL) A shift register as claimed in claim 17, wherein said first resistor element is a transistor.

19. (CURRENTLY AMENDED) A shift register as claimed in claim 17, wherein ~~said second resistor elements is~~ element are inserted ~~respectively~~ between ~~the~~ a power supply and each of the two input sections of the CMOS latch cell.

20. (ORIGINAL) A shift register as claimed in claim 19, wherein said first and said second resistor elements are transistors.

21. (CURRENTLY AMENDED) A shift register as claimed in claim 19, wherein level shift operation is performed only when said a switch is in an on status by utilizing switches having a finite resistance value as said first and said second resistor elements, and at all other times latch operation is performed.

22. (CURRENTLY AMENDED) A shift register as claimed in claim 21, wherein said shift register has a control circuit to set said switch to the on status only when necessary.

23. (CURRENTLY AMENDED) A shift register as claimed in claim 21, wherein said shift register has a reset circuit to determine ~~the~~ initial status of said CMOS latch cell.

24. (ORIGINAL) A shift register as claimed in claim 17, wherein said shift register is fabricated utilizing thin film transistors formed on a glass substrate.

25. (ORIGINAL) A shift register as claimed in claim 17, wherein said shift register is fabricated utilizing thin film transistors formed on a silicon substrate.

26. (CANCELED).

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40. (Amended) A sampling latch circuit with comprising:
a comparator configuration CMOS latch cell as the basic structure and
comprising having two input sections;

a first switch connected ~~respectively~~ between each of the two input sections and ~~the two input signal sources of said CMOS latch cell and;~~
a second switch connected between ~~the~~ a power supply line and ~~the~~ a power supply side of said CMOS latch cell; and,
a control means to control ~~the~~ complementary switching of said first switch and said second switch.

41. (ORIGINAL) A sampling latch circuit as claimed in claim 40, wherein said first switch and said second switch are transistors.

42. (ORIGINAL) A sampling latch circuit as claimed in claim 40, wherein a plurality of said sampling latch circuits are installed and, said second switch is jointly shared by said plurality of sampling latch circuits.

43. (CURRENTLY AMENDED) A sampling latch circuit as claimed in claim 40 also having further comprising:

a third switch, synchronized and controlled by said second switch, between the power supply line and ~~the~~ a power supply side of ~~the~~ an output circuit for output of said CMOS latch circuit output signal.

44. (ORIGINAL) A sampling latch circuit as claimed in claim 43, wherein said second switch is combined with said third switch.

45. (ORIGINAL) A sampling latch circuit as claimed in claim 44, wherein a plurality of said sampling latch circuits are installed and, said second switch is jointly shared by said plurality of sampling latch circuit.

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54. (CURRENTLY AMENDED) A latch circuit ~~with~~ including a CMOS latch cell having two input sections as a basic structure, wherein said latch circuit has comprising a first switch and a second switch to respectively select a first and second power supply having different voltages and installed on at least one of the a positive power side or ~~the~~ a negative power side of said CMOS latch cell and, having a control means to control switching of said first and second switches according to ~~the periods of the~~ a latch operation period and an output operation period of said CMOS latch cell.

55. (ORIGINAL) A latch circuit as claimed in claim 54, wherein said first and second switches are transistors.

56. (ORIGINAL) A latch circuit as claimed in claim 54, wherein a plurality of said latch circuits are installed and, said first switch and said second switch are jointly shared by said plurality of sampling latch circuits.

57. (ORIGINAL) A latch circuit as claimed in claim 54, wherein said latch circuit is fabricated by utilizing thin film transistors formed on a glass substrate.

58 (ORIGINAL) A latch circuit as claimed in claim 54, wherein said latch circuit is fabricated by utilizing thin film transistors formed on a silicon substrate.